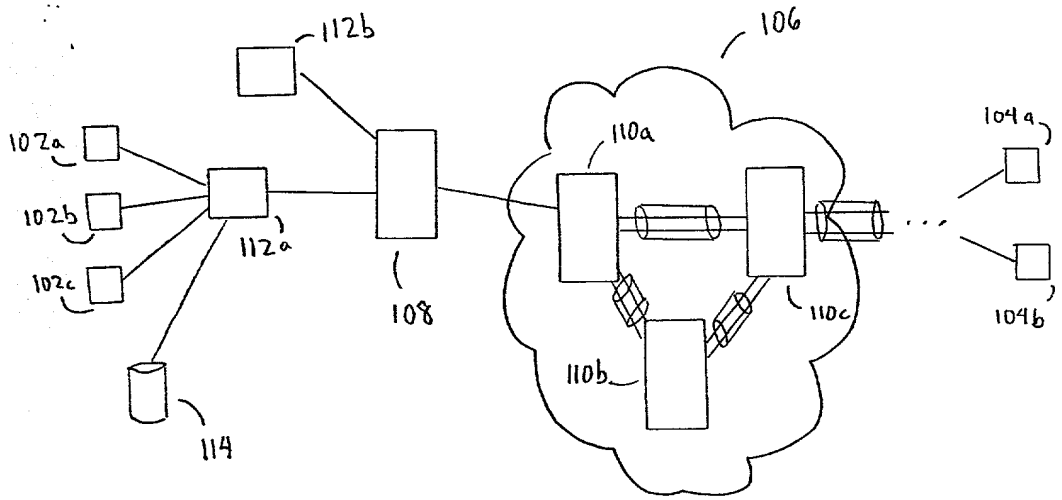
Fig. 1



100

Fig. 2a

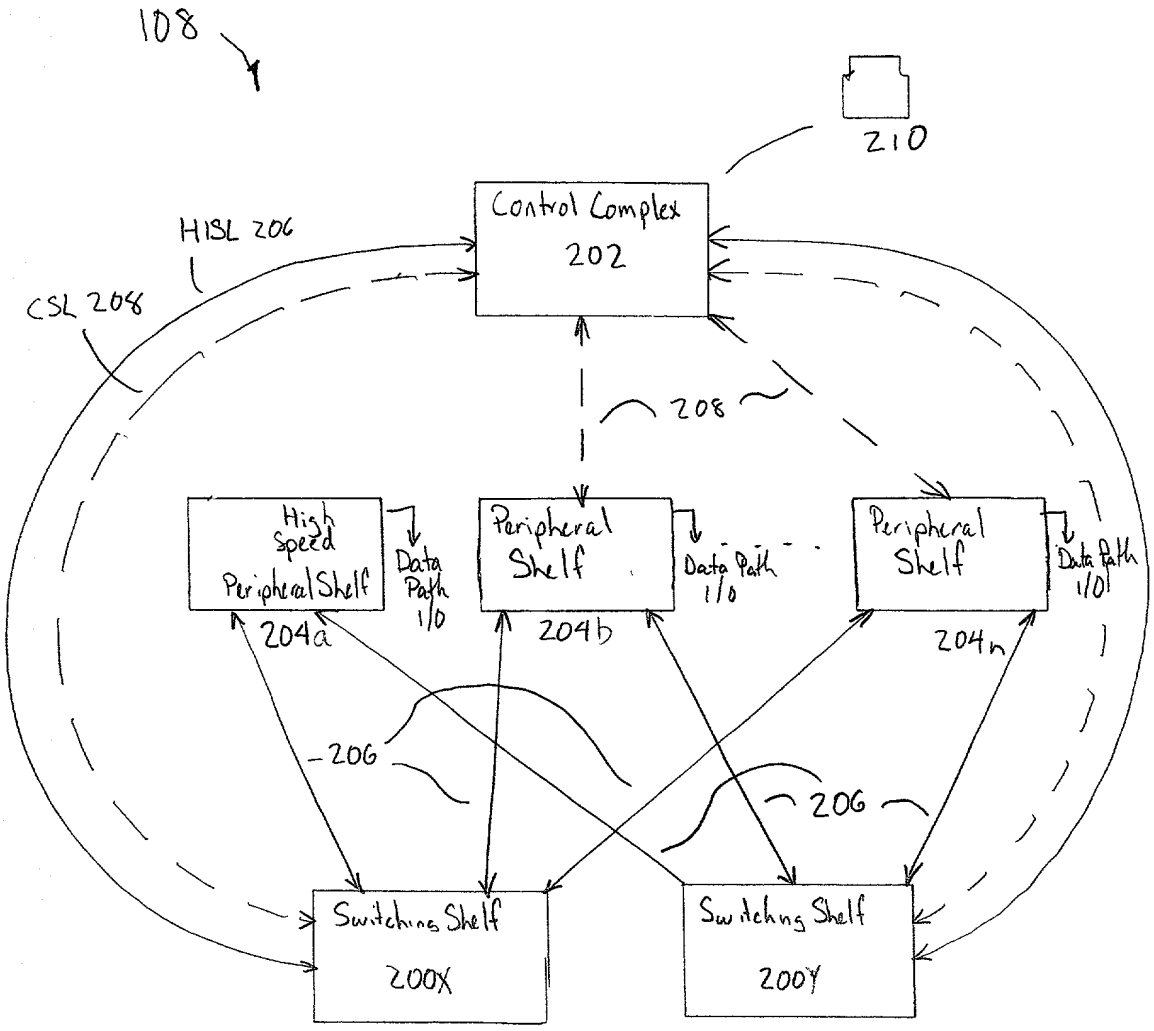

108
210
Control Complex
202
HISL 206
CSL 208
208
High Speed Peripheral Shelf
Data Path I/O
204a
Peripheral Shelf
Data Path I/O
204b
Peripheral Shelf
Data Path I/O
204n
206
206
Switching Shelf
200X
Switching Shelf
200Y

Fig 2B

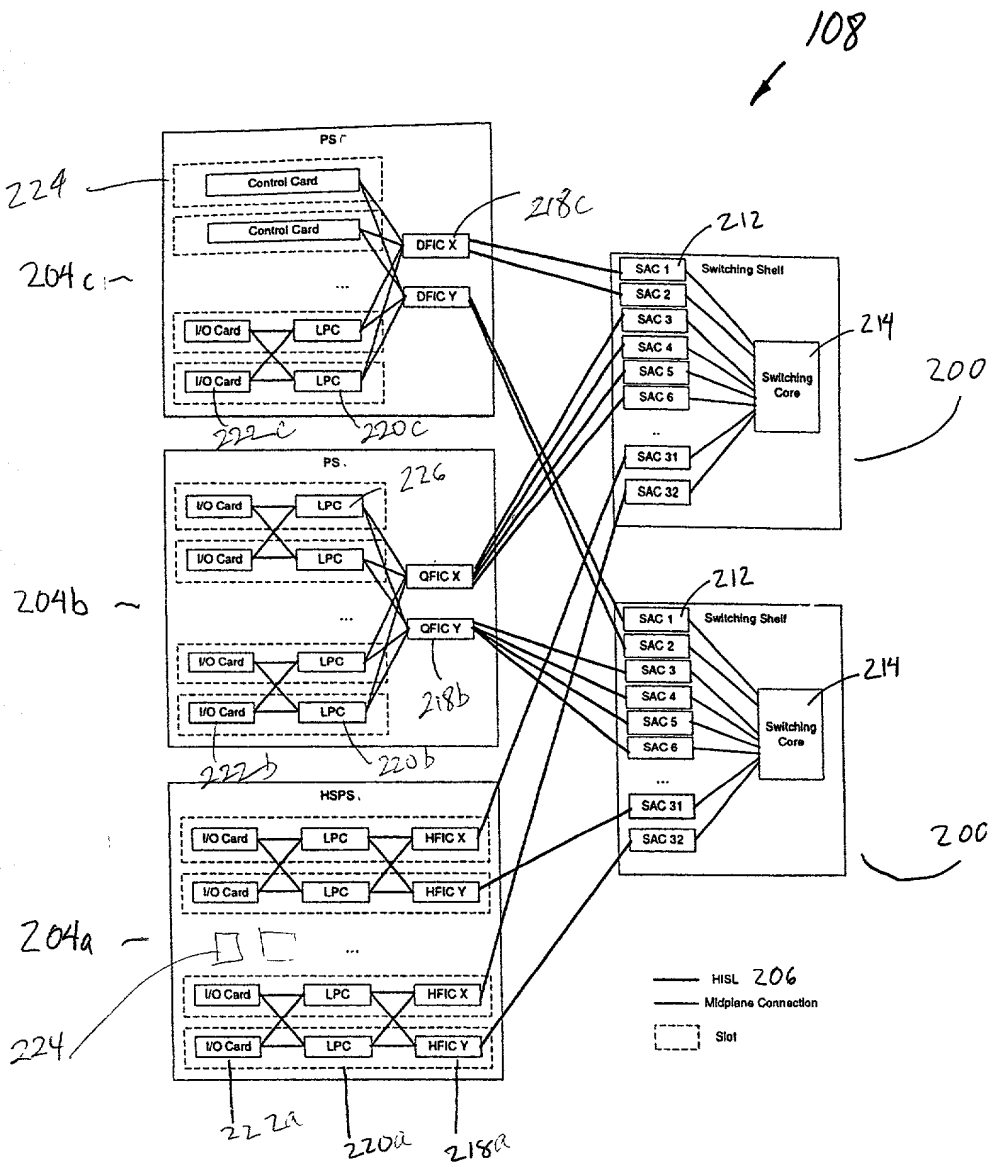
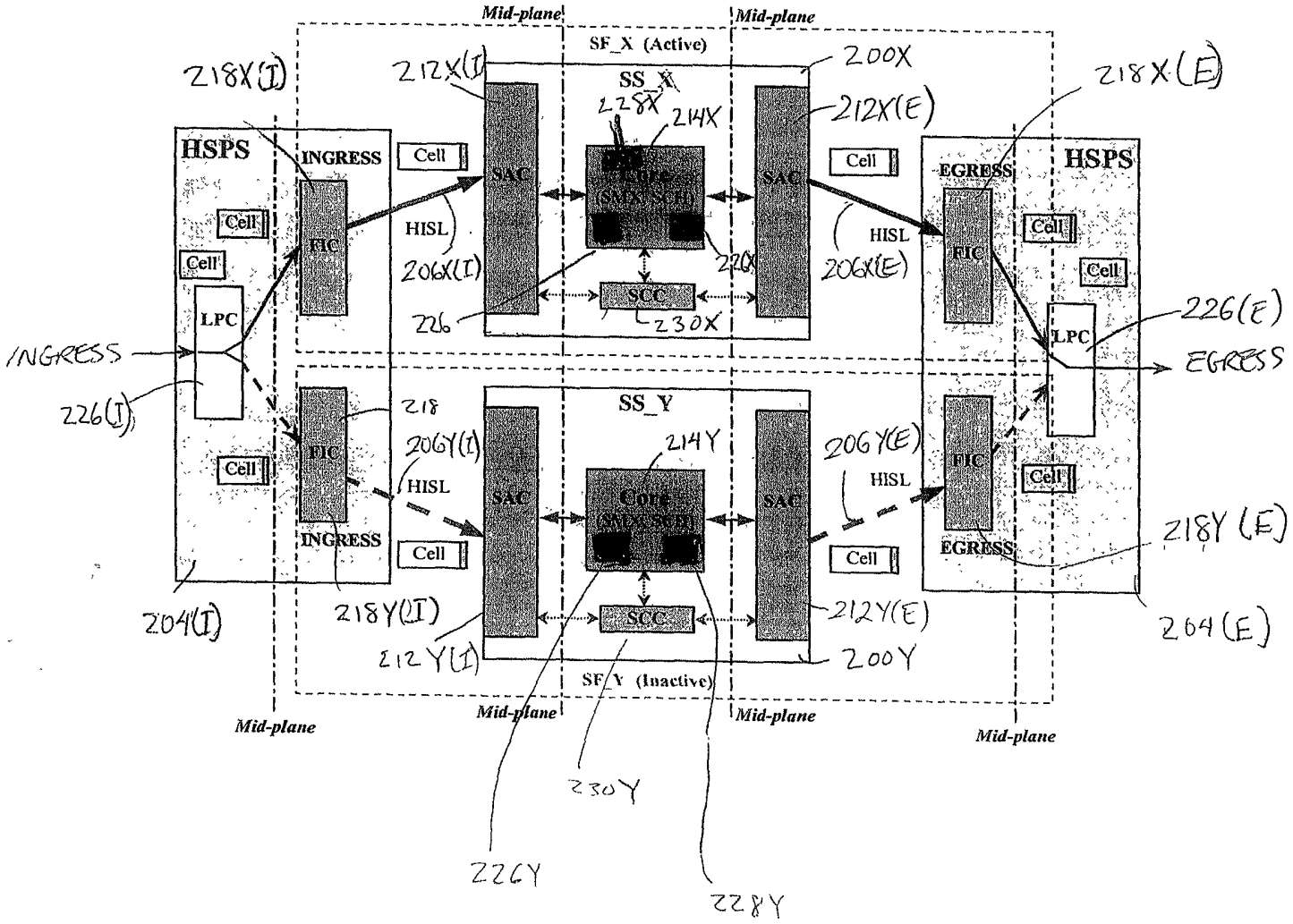

108
224
204c
218c
212
DFIC X
DFIC Y
Control Card
Control Card
I/O Card
LPC
I/O Card
LPC
222c
220c
PS
SAC 1
SAC 2
SAC 3
SAC 4
SAC 5
SAC 6
SAC 31
SAC 32
Switching Shelf
Switching Core
214
200
226
204b
QFIC X
QFIC Y
218b
222b
220b
HSPS
HFIC X
HFIC Y
204a
224
222a
220a
218a
206
HISL
Midplane Connection
Slot

Fig. 2C


Mid-plane
Mid-plane
SF_X (Active)
SS_X
218X(I)
212X(I)
200X
212X(E)
218X(E)
HSPS
INGRESS
Cell
SAC
Core
SCC
SAC
Cell
EGRESS
HSPS
Cell
Cell
FIC
HISL
206X(I)
220X
206X(E)
FIC
Cell
Cell
LPC
LPC
226
230X
226(E)
INGRESS
EGRESS
226(I)
218
206Y(I)
214Y
206Y(E)
HISL
FIC
HISL
FIC
Cell
Cell
SS_Y
SAC
Core
SAC
Cell
EGRESS
INGRESS
Cell
218Y(E)
204(I)
218Y(I)
212Y(I)
SCC
212Y(E)
200Y
204(E)
SF_Y (Inactive)
Mid-plane
Mid-plane
Mid-plane
Mid-plane
230Y
226Y
228Y

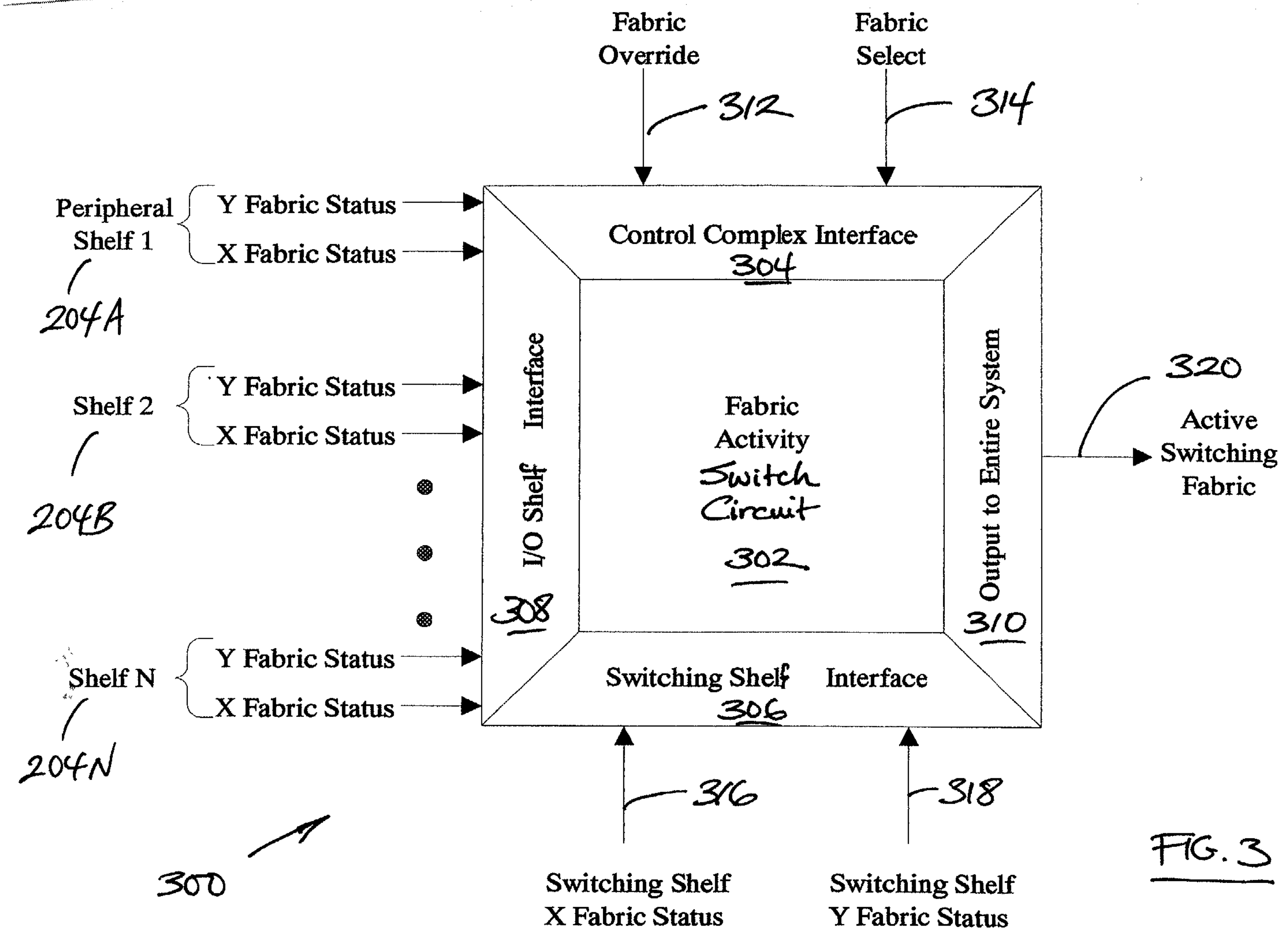

Fabric Override
312
Fabric Select
314
Peripheral Shelf 1
204A
Y Fabric Status
X Fabric Status
Shelf 2
204B
Y Fabric Status
X Fabric Status
Shelf N
204N
Y Fabric Status
X Fabric Status
Control Complex Interface
304
I/O Shelf Interface
308
Fabric Activity Switch Circuit
302
Output to Entire System
310
Switching Shelf Interface
306
320
Active Switching Fabric
316
318
Switching Shelf X Fabric Status
Switching Shelf Y Fabric Status
300

FIG. 3

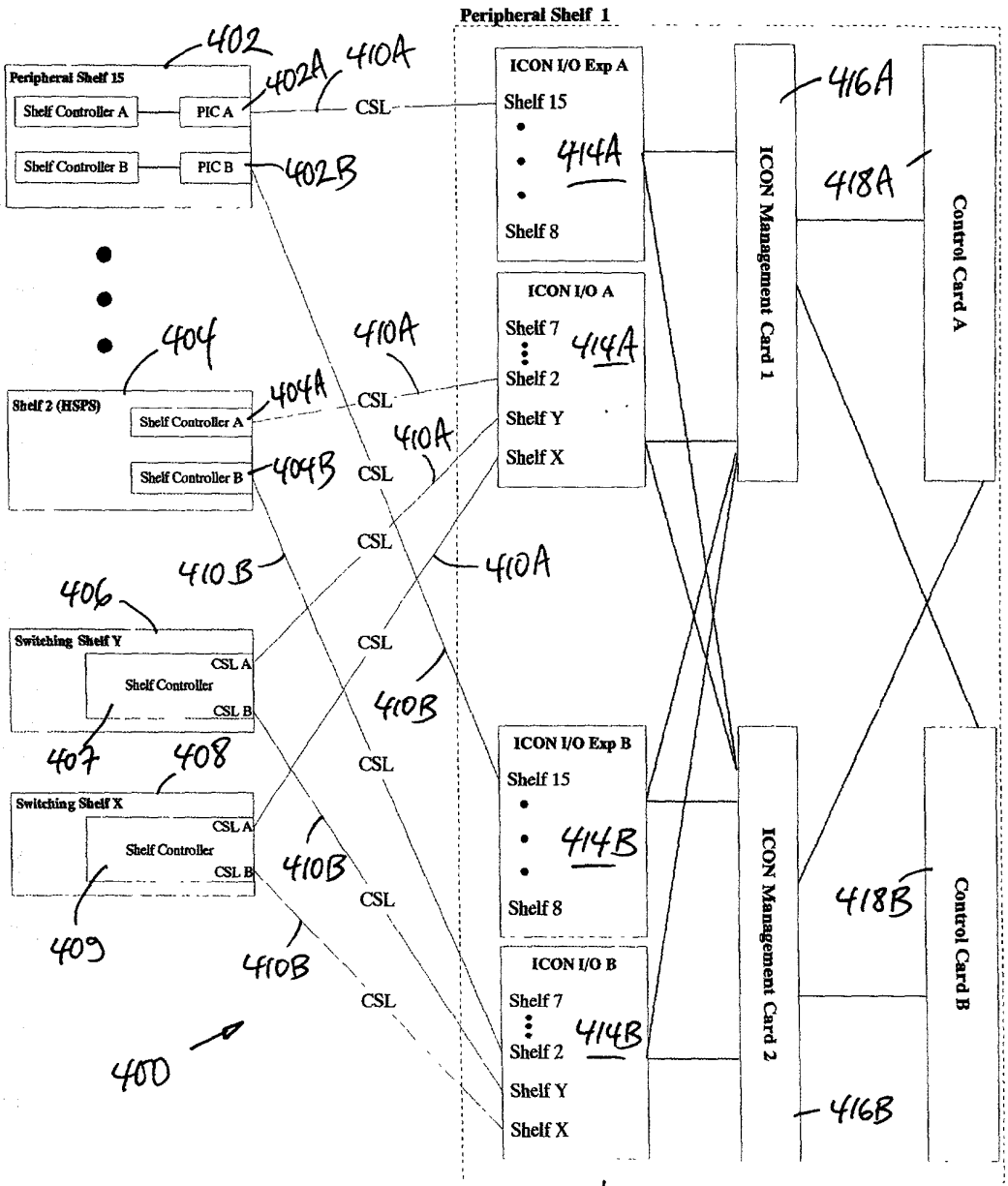

Peripheral Shelf 1
402
Peripheral Shelf 15
Shelf Controller A
PIC A
402A
410A
CSL
Shelf Controller B
PIC B
402B
ICON I/O Exp A
Shelf 15
414A
Shelf 8
ICON Management Card 1
416A
418A
Control Card A
404
Shelf 2 (HSPS)
Shelf Controller A
404A
Shelf Controller B
404B
ICON I/O A
Shelf 7
Shelf 2
Shelf Y
Shelf X
410B
406
Switching Shelf Y
CSL A
Shelf Controller
CSL B
407
408
Switching Shelf X
409
ICON I/O Exp B
ICON I/O B
ICON Management Card 2
418B
Control Card B
416B
400
412

FIG. 4

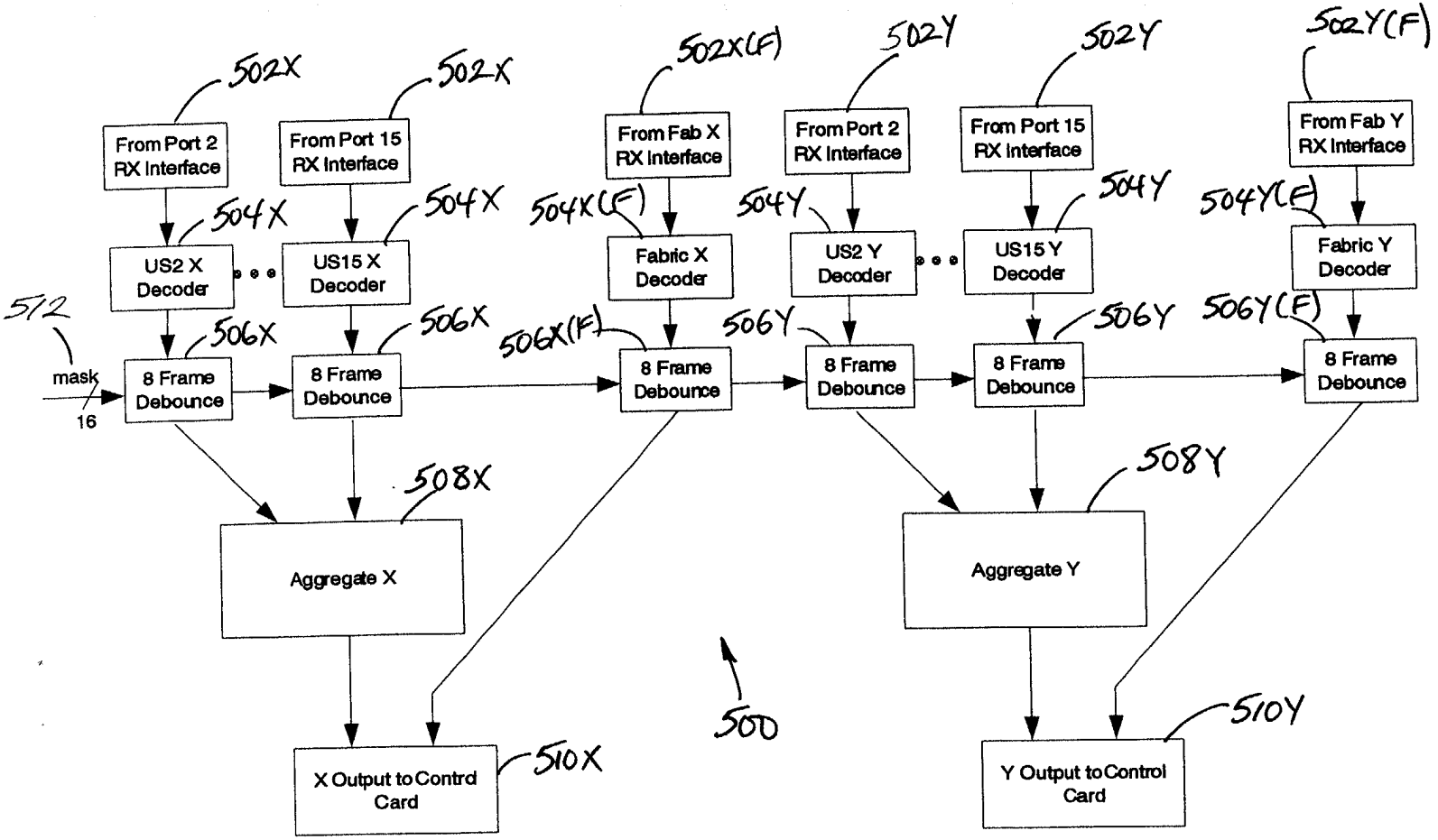

502X
502X
502X(F)
502Y
502Y
502Y(F)
From Port 2 RX Interface
From Port 15 RX Interface
From Fab X RX Interface
From Port 2 RX Interface
From Port 15 RX Interface
From Fab Y RX Interface
504X
504X
504X(F)
504Y
504Y
504Y(F)
US2 X Decoder
US15 X Decoder
Fabric X Decoder
US2 Y Decoder
US15 Y Decoder
Fabric Y Decoder
512
mask
16
506X
506X
506X(F)
506Y
506Y
506Y(F)
8 Frame Debounce
8 Frame Debounce
8 Frame Debounce
8 Frame Debounce
8 Frame Debounce
8 Frame Debounce
508X
508Y
Aggregate X
Aggregate Y
500
510X
510Y
X Output to Contrd Card
Y Output to Control Card

FIG. 5

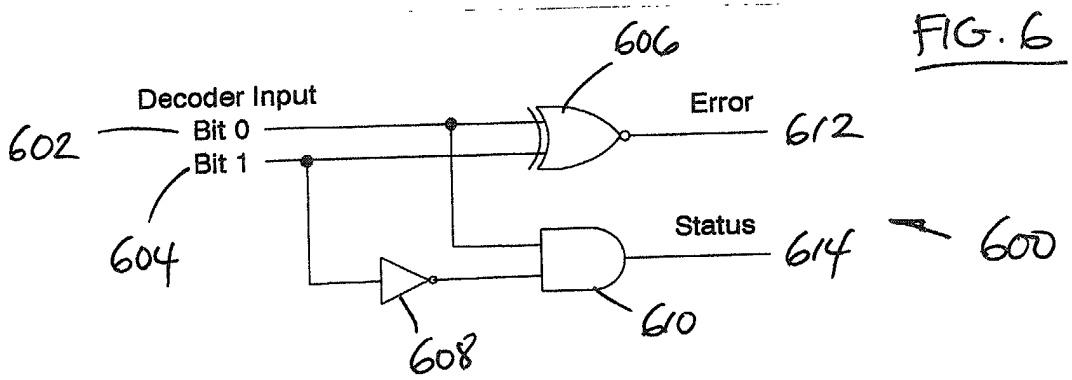
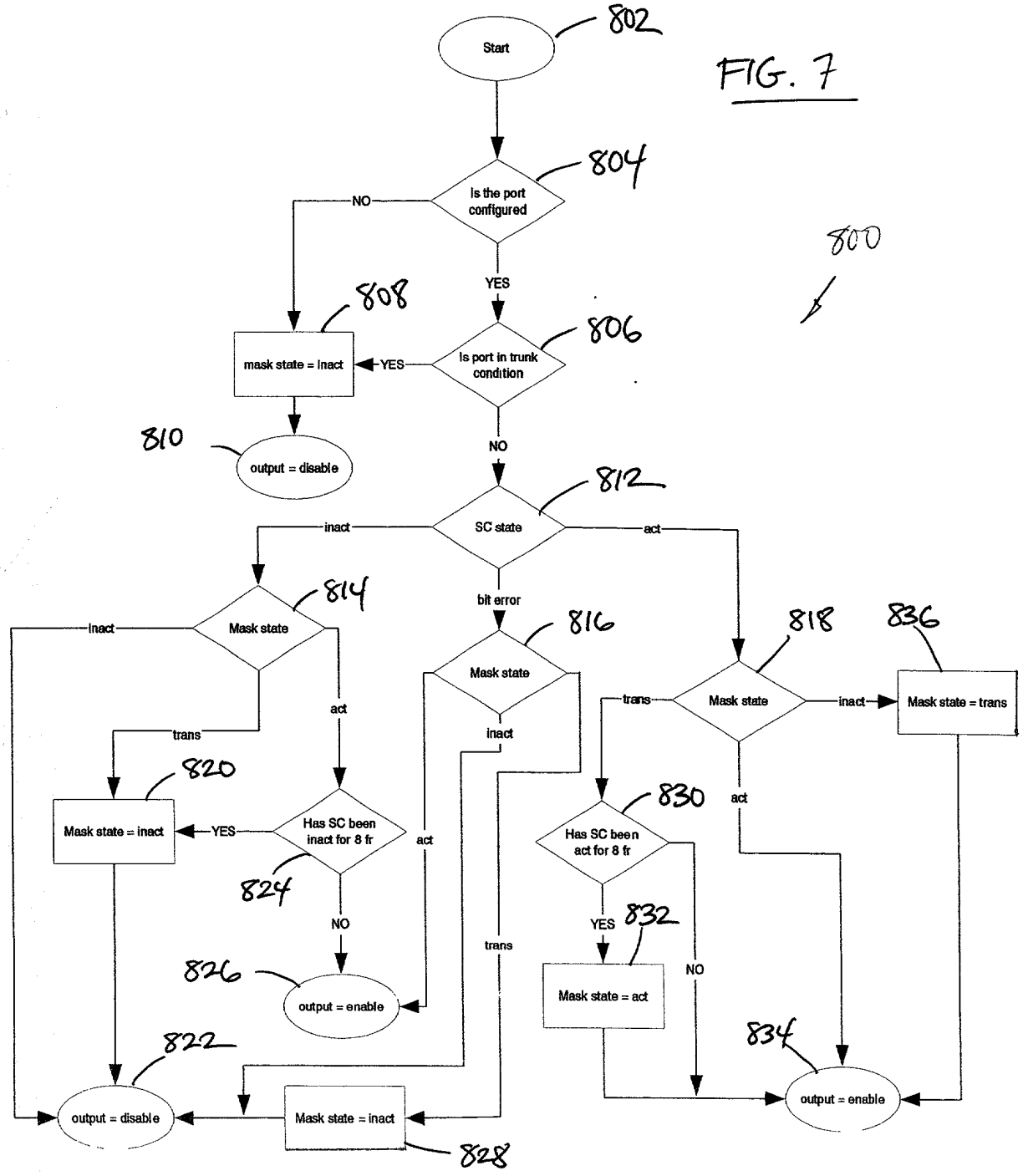


FIG. 6

FIG. 7


800
802
Start
804
Is the port configured
NO
YES
806
Is port in trunk condition
808
mask state = Inact
YES
810
output = disable
NO
812
SC state
inact
act
bit error
814
Mask state
Inact
trans
act
820
Mask state = inact
YES
Has SC been inact for 8 fr
824
NO
826
output = enable
822
output = disable
816
Mask state
inact
act
trans
Mask state = inact
828
818
Mask state
trans
inact
act
836
Mask state = trans
830
Has SC been act for 8 fr
YES
832
Mask state = act
NO
834
output = enable

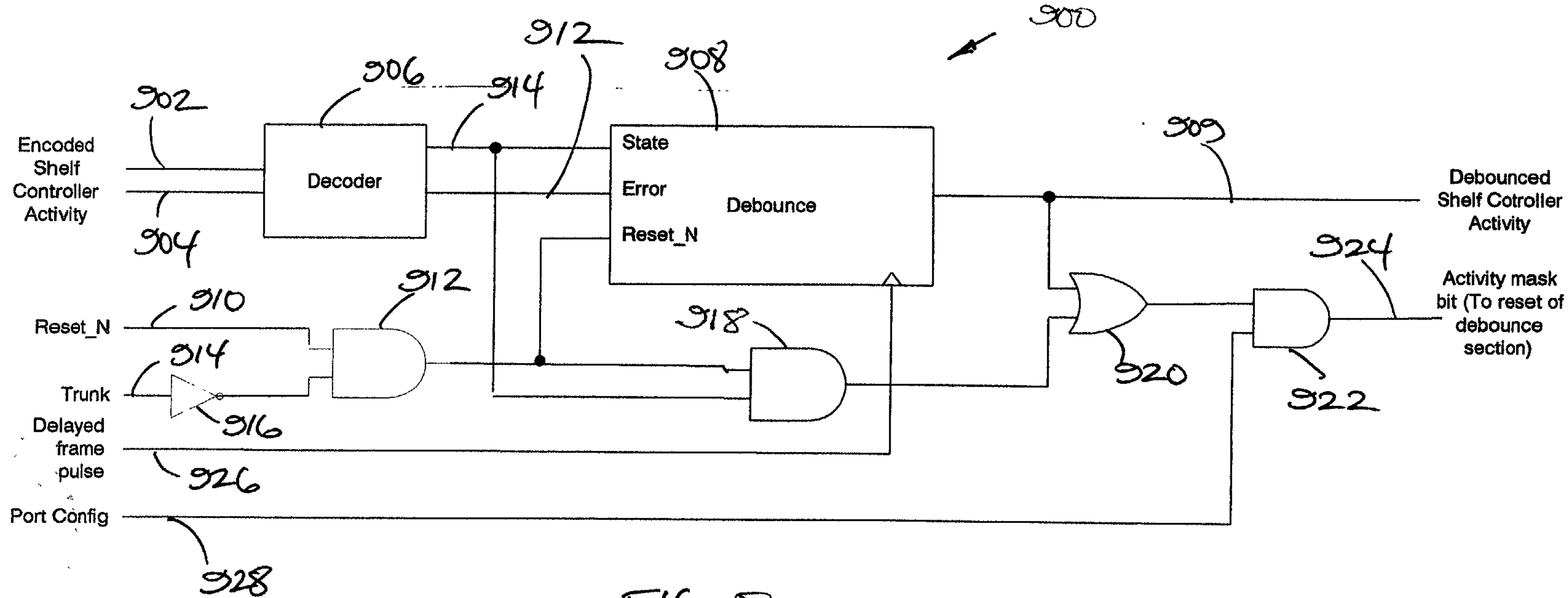

900
902
904
906
908
909
910
912
914
916
918
920
922
924
926
928
Encoded Shelf Controller Activity
Decoder
State
Error
Reset_N
Debounce
Reset_N
Trunk
Delayed frame pulse
Port Config
Debounced Shelf Cotroller Activity
Activity mask bit (To reset of debounce section)

FIG. 8

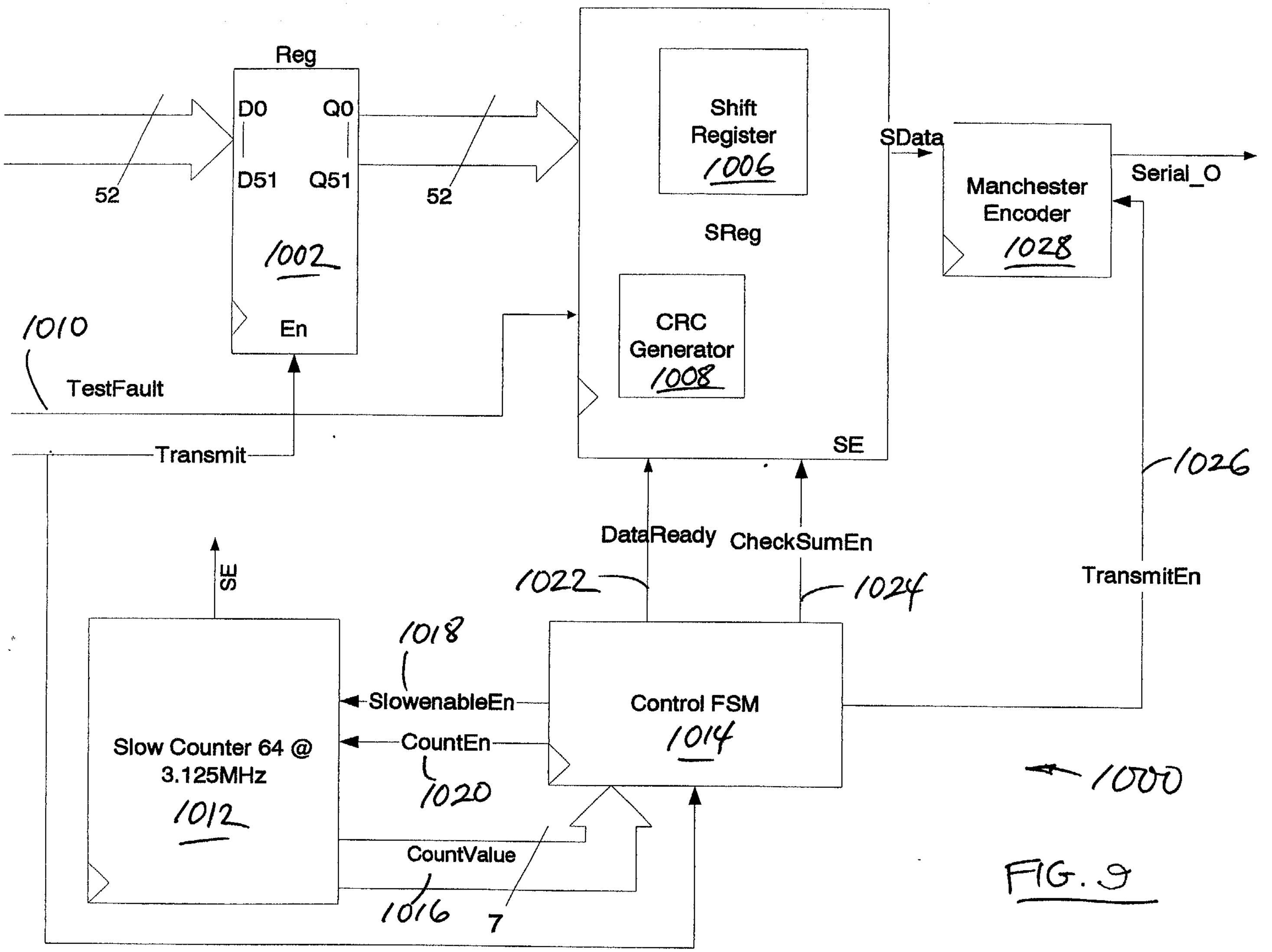

Reg
D0
D51
Q0
Q51
52
52
1002
En
1010
TestFault
Transmit
Shift Register
1006
SReg
CRC Generator
1008
SE
SData
Manchester Encoder
1028
Serial_O
1026
TransmitEn
DataReady
CheckSumEn
1022
1024
SE
Slow Counter 64 @ 3.125MHz
1012
1018
SlowenableEn
CountEn
1020
Control FSM
1014
CountValue
1016
7
1000

FIG. 9

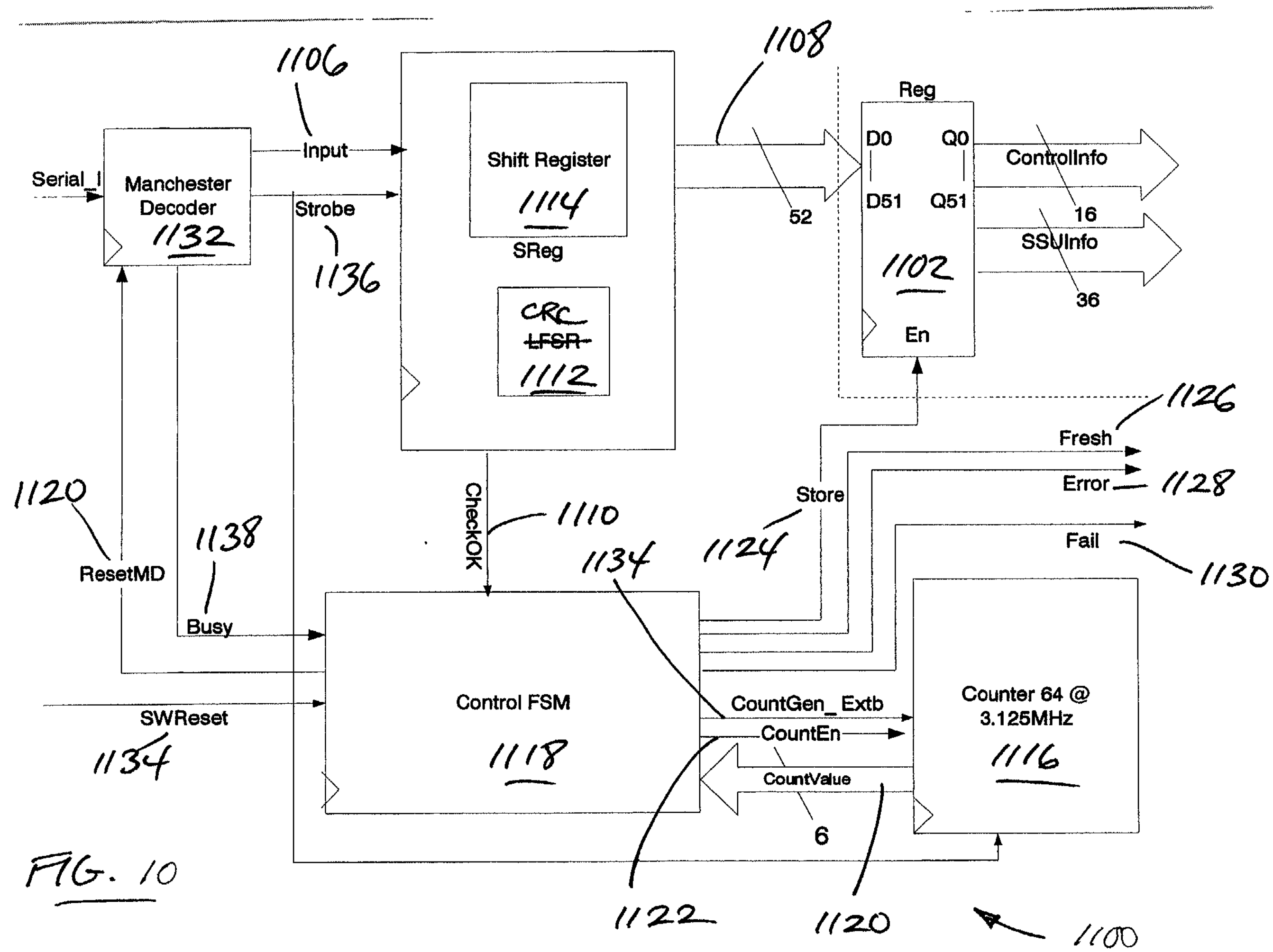

Serial_I
Manchester Decoder
1132
Input
Strobe
1106
1136
Shift Register
1114
SReg
CRC
LFSR
1112
1108
52
Reg
D0
D51
Q0
Q51
1102
En
ControlInfo
16
SSUInfo
36
CheckOK
1110
Fresh
1126
Error
1128
Fail
1130
Store
1124
1120
ResetMD
1138
Busy
SWReset
1134
Control FSM
1118
CountGen_Extb
CountEn
CountValue
6
Counter 64 @ 3.125MHz
1116
1122
1120
1100

FIG. 10

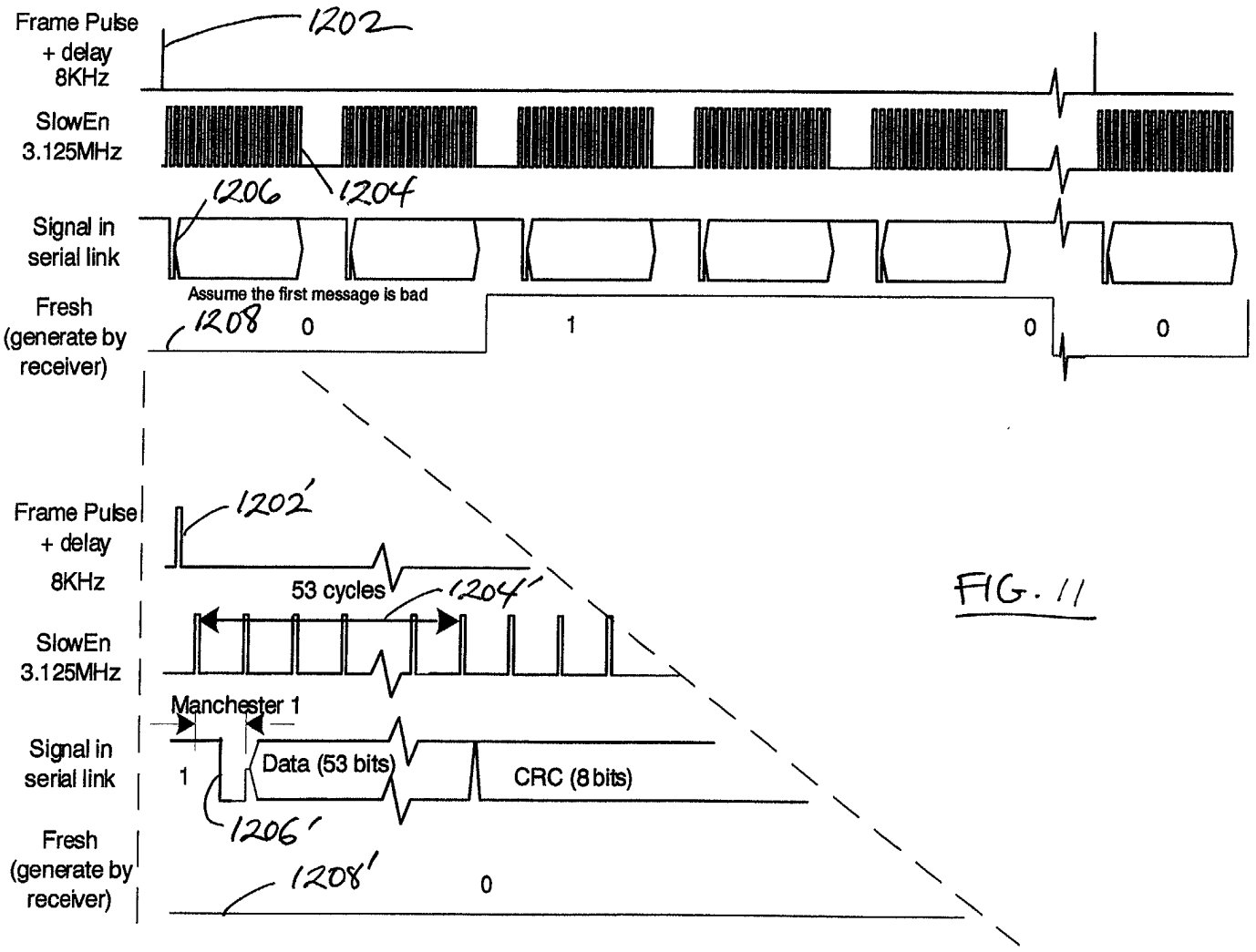


FIG. 11

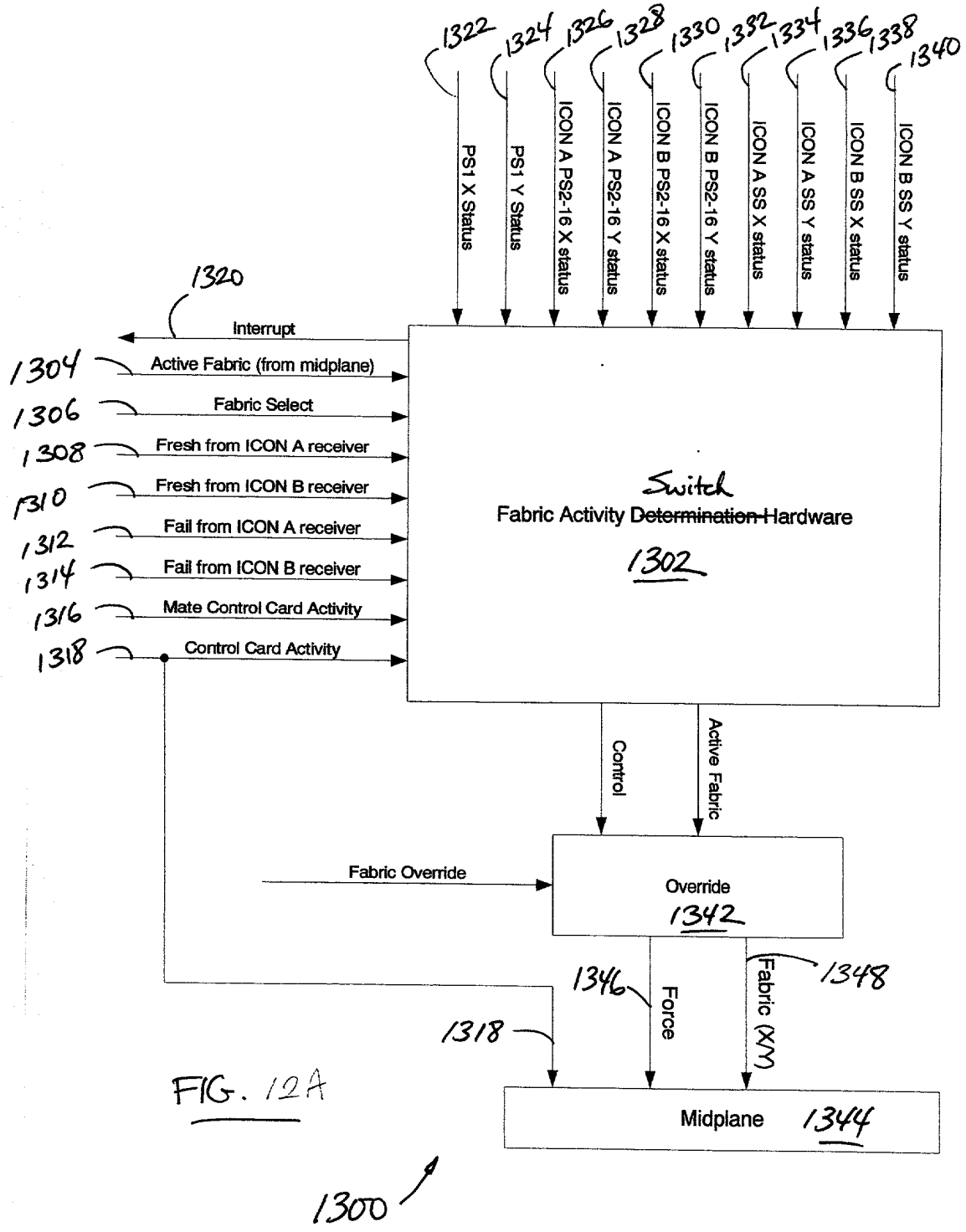

1322
1324
1326
1328
1330
1332
1334
1336
1338
1340
PS1 X Status
PS1 Y Status
ICON A PS2-16 X status
ICON A PS2-16 Y status
ICON B PS2-16 X status
ICON B PS2-16 Y status
ICON A SS X status
ICON A SS Y status
ICON B SS X status
ICON B SS Y status
1320
Interrupt
1304
Active Fabric (from midplane)
1306
Fabric Select
1308
Fresh from ICON A receiver
1310
Fresh from ICON B receiver
1312
Fail from ICON A receiver
1314
Fail from ICON B receiver
1316
Mate Control Card Activity
1318
Control Card Activity
Switch
Fabric Activity Determination Hardware
1302
Control
Active Fabric
Fabric Override
Override
1342
1346
Force
1348
Fabric (X/Y)
1318
Midplane
1344
1300

FIG. 12A

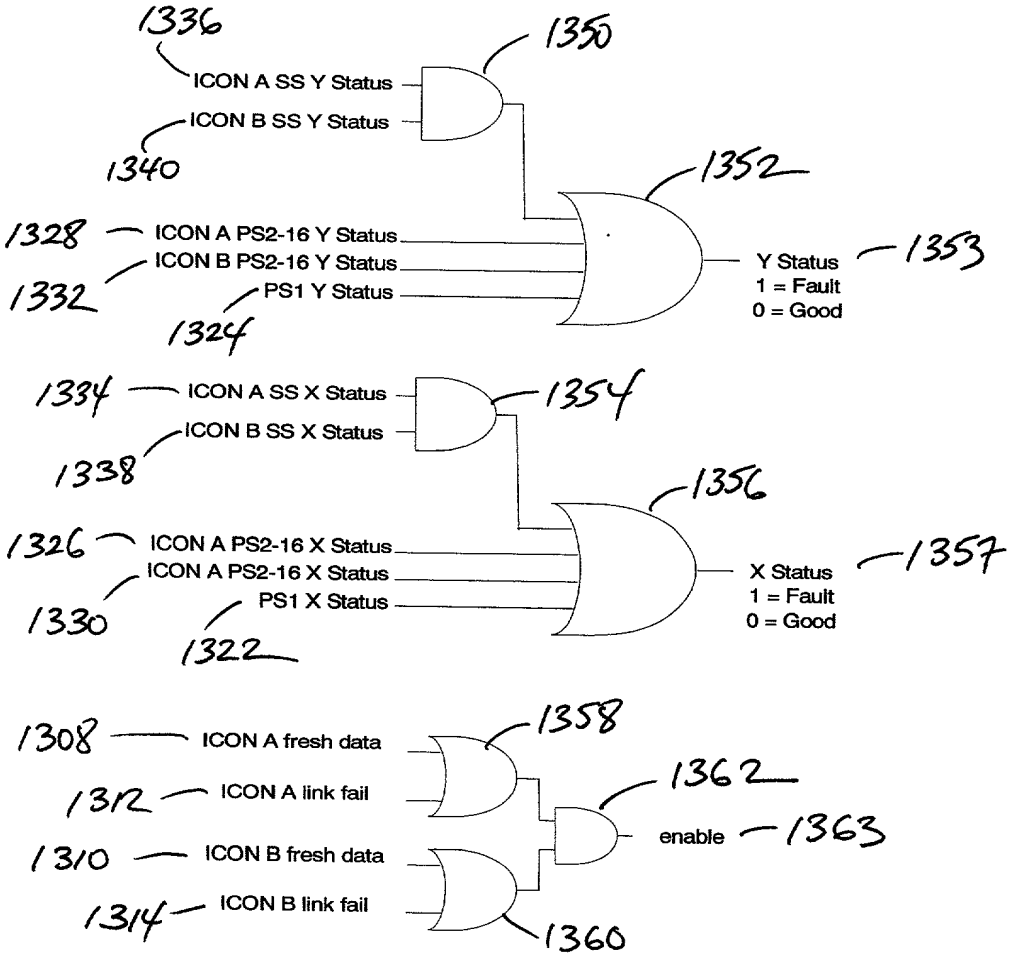

1336
1350
ICON A SS Y Status
ICON B SS Y Status
1340
1352
1328
ICON A PS2-16 Y Status
ICON B PS2-16 Y Status
1332
PS1 Y Status
1324
Y Status
1 = Fault
0 = Good
1353
1334
ICON A SS X Status
1354
ICON B SS X Status
1338
1356
1326
ICON A PS2-16 X Status
ICON A PS2-16 X Status
1330
PS1 X Status
1322
X Status
1 = Fault
0 = Good
1357
1308
ICON A fresh data
1358
1312
ICON A link fail
1362
enable
1363
1310
ICON B fresh data
1314
ICON B link fail
1360

FIG. 12B

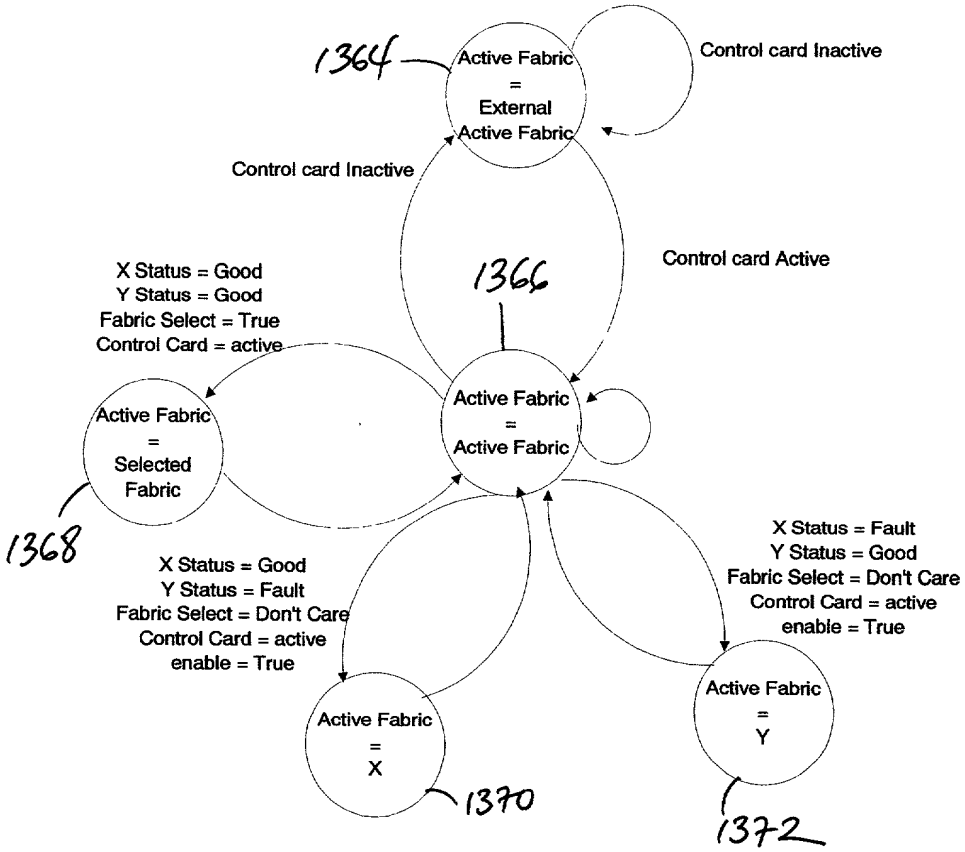

1364
Active Fabric
=
External
Active Fabric
Control card Inactive
Control card Inactive
1366
Control card Active
X Status = Good
Y Status = Good
Fabric Select = True
Control Card = active
Active Fabric
=
Selected
Fabric
1368
Active Fabric
=
Active Fabric
X Status = Good
Y Status = Fault
Fabric Select = Don't Care
Control Card = active
enable = True
X Status = Fault
Y Status = Good
Fabric Select = Don't Care
Control Card = active
enable = True
Active Fabric
=
X
1370
Active Fabric
=
Y
1372

FIG. 12C

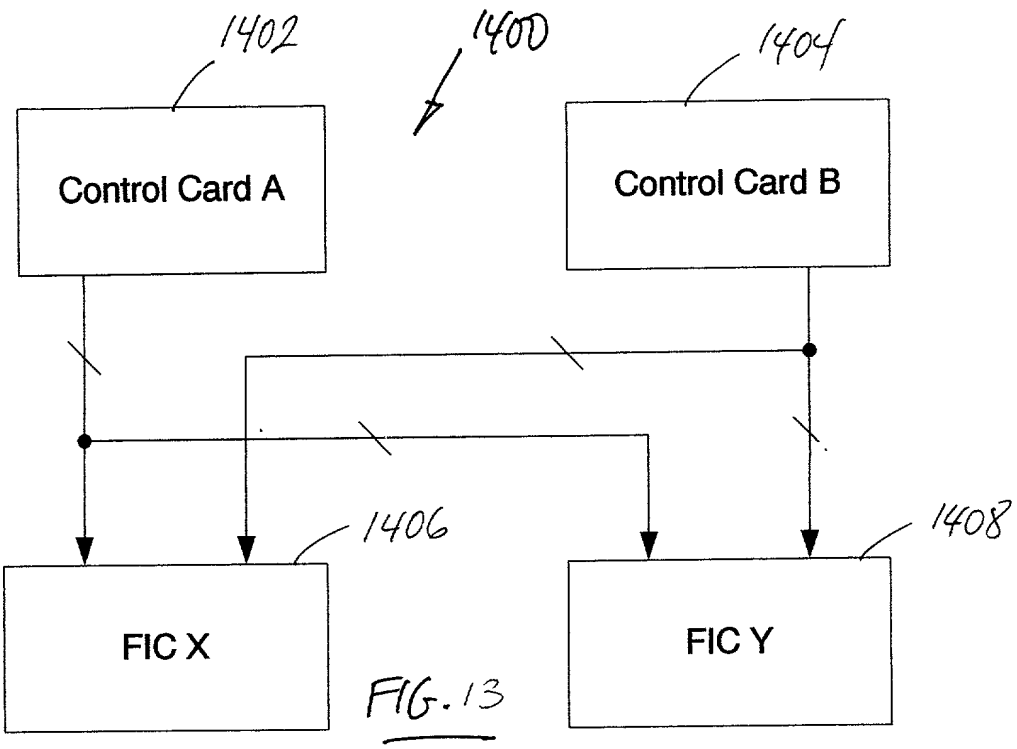

1402
1400
1404
Control Card A
Control Card B
1406
1408
FIC X
FIC Y

FIG. 13

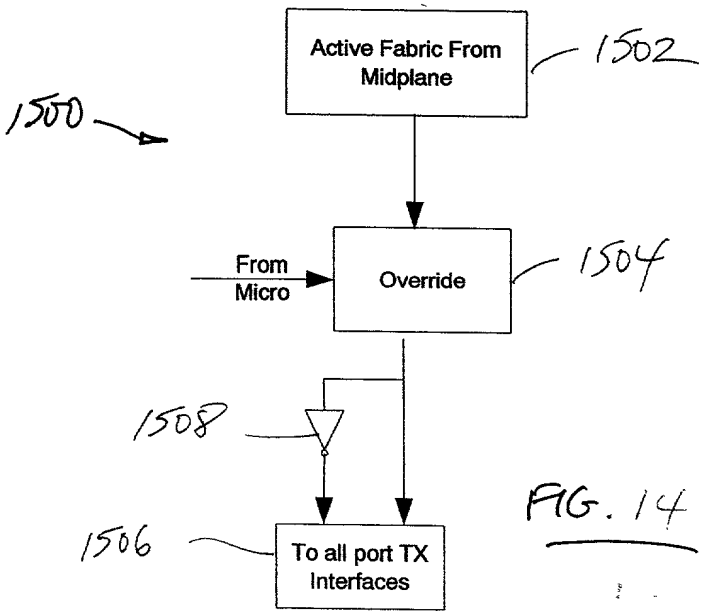

1500
Active Fabric From Midplane
1502
From Micro
Override
1504
1508
1506
To all port TX Interfaces

FIG. 14